first direction, said first to third edges forming a step shape so that the second edge is depressed toward an inside of said active area beyond the first edge;

designing a layout of a first gate electrode of a first MOS transistor on said active area, one end of said first gate electrode extending to an outside of said active area across the first edge in a vertical direction to the first direction, and

designing a layout of a second gate electrode of a second MOS transistor on said active area, one end of said second gate electrode extending to an outside of said active area across the second edge in a vertical direction to the first direction,

wherein a length from the second edge to the one end of said second gate electrode is longer than a length from the first edge to the one end of said first gate electrode.--

REMARKS

This amendment responds to the Office Action dated April 6, 2000, in which the Examiner rejected claim 1 under 35 U.S.C. §102(e).

Applicants respectfully request the Examiner acknowledge receiving the priority document filed September 25, 1998.

Claim 1 claims a semiconductor device comprising an active area and an insulating film. The active area is provided with at least one MOS transistor. The insulating film defines the active area. The active area is set in a shape having a concave part in a shape along a plan view. The active area is provided with an ordinary region and a depressed region having an edge portion which is depressed beyond the ordinary region due to the presence of the concave part. The at least one MOS transistor includes first and second

MOS transistors. The first MOS transistor is formed in the depressed region. The second MOS transistor is formed on the ordinary region. A length of a margin part of a first gate electrode constructing the first MOS transistor is set to be larger than that of a margin part of a second gate electrode constructing the second MOS transistor.

Through the structure of the present invention having first and second MOS transistors, each having a margin part and where the length of the margin part of the first gate electrode is larger than that of the margin part of the second gate electrode, as claimed in claim 1, the present invention provides a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length and therefore prevents occurrence of current leakage between source/drain regions which are formed on the exterior of both side surfaces of the first gate electrode. The prior art does not show, teach or suggest first and second MOS transistors each having a margin part where the length of the margin part of the first gate electrode of the first transistor is larger than the margin part of the second gate electrode of the second transistor as claimed in claim 1.

Applicants respectfully submit that claim 1 is generic to the species depicted in Figures 24-27.

As indicated above, claim 1 has been amended only to correct a formal matter. Therefore, it is respectfully requested that the Examiner approves the correction.

Claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by *Shou et al.* (U.S. Patent No. 5,811,859).

Applicants respectfully traverse the Examiner's rejection of the claim under 35 U.S.C. §102(e). The claim has been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claim and allows the claim to issue.

Shou et al. appears to disclose a LSI pattern of inverted amplifier INV consisting of three stages MOS inverters I1, I2 and I3. For the inverters I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for input from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. A strangulation portion S1 is provided between the contacts C1 and C5 in the semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. The strangulation means S1 limit an electric current in the output of the inverter I2, and it simultaneously decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency.

Thus, *Shou et al.* merely discloses a first gate G passing through a strangulation portion and a second gate G ending at the end of the P-type semiconductor layer PL1. Thus, nothing in *Shou et al.* shows, teaches or suggests that the gate electrode of the second transistor formed in the ordinary region has a margin part as claimed in claim 1. Rather, *Shou et al.* teaches away from the present invention since Figure 3 of *Shou et al.* clearly discloses that the gate electrode ends at the end of the common P-type

semiconductor layer PL1 (i.e., the gate does not protrude from PL1). Thus, nothing in *Shou et al.* discloses a margin part for the transistor in the ordinary region as claimed in claim 1.

Additionally, since nothing in *Shou et al.* shows, teaches or suggests a margin part of a second gate electrode of the transistor in the ordinary region, nothing in *Shou et al.* shows, teaches or suggests that a margin part of a first gate electrode of the transistor formed on the depressed region is larger than the margin part of the gate electrode of the transistor formed on the ordinary region as claimed in claim 1. Rather, *Shou et al.* teaches away from the present invention and merely discloses a gate electrode of a transistor formed on a strangulation region has a margin part while the gate electrode of the transistor formed on the common P-type semiconductor region has no margin part (i.e., *Shou et al.* does not teach a margin part for each transistor gate).

Since nothing in *Shou et al.* shows, teaches or suggests a) a transistor formed on an ordinary region having a gate electrode having a margin part or b) a length of a margin part of a gate electrode of a transistor formed on a depressed region is larger than a margin part of a gate electrode of a transistor formed on an ordinary region, as claimed in claim 1, it is respectfully requested that the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(e).

Claims 2-5 depend from generic claim 1. Therefore, it is respectfully requested that these claims should no longer be withdrawn. It is respectfully requested that these claims be allowed.

As indicated above, claim 12 has been added. It is respectfully submitted that claim 12 is generic and should be allowed.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If, for any reason, the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contacts, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fee for such an extension of time may be charged to our Deposit Account 02-4800.

In the event that any additional fees are due with this paper, please just charge our Deposit Account 02-4800.

Respectfully submitted,

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